REMARKS/ARGUMENTS

This Amendment is in response to the Office Action mailed March 27, 2006. Claims 27-40 were pending in the present application. This Amendment amends claims 27, 31, and 36, without adding or canceling any claims, leaving pending in the application claims 27-40. Reconsideration of the rejected claims is respectfully requested.

I. Objection of the Abstract

The abstract of the disclosure is objected to as failing to reflect the inventive nature of the claimed invention. Applicants respectfully disagree with the rejection, but have amended the abstract to more closely reflect the current state of the claims in order to advance prosecution. Applicants submit that the abstract distinguishes over the prior art, for reasons including those set forth below, and respectfully request that the rejection with respect to the abstract be withdrawn.

II. Rejection under 35 U.S.C. §112

Claims 27-40 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, claims 27, 31, and 37 are rejected as improperly reciting that the data length is equal to the instruction length. Although Applicants disagree with the rejection, the claims as amended no longer recite the limitation that was rejected, such that the rejection is now moot.

Claims 29, 34, and 36 are rejected for the unclear use of the term "pre-decode signal." Applicants respectfully disagree with the rejection, as the specification clearly sets out and defines a pre-decode signal. Further, claim 36, for example, recites a pre-decoder circuit and a decoder circuit, each operable to perform a function, where the decoder circuit receives a pre-decode signal produced by the pre-decode circuit. It is respectfully submitted that such limitations are clear and definite, and there should be no

problem with the claims referring to a circuit as a pre-decode circuit that produces a pre-decode signal before the signal reaches a decode circuit.

Applicants therefore respectfully request that the rejection with respect to claims 27-40 be withdrawn.

III. Rejection under 35 U.S.C. §102

Claims 27-40 are rejected under 35 U.S.C. §102(b) as being anticipated by *Jaggar* (US 5,568,646). Applicants respectfully submit that *Jaggar* does not disclose each element of these claims.

For example, Applicants' claim 27 as amended recites a data processing unit, comprising:

> an instruction cache to store instructions for execution, including instructions belonging to an M-bit instruction set and instructions belonging to an N-bit instruction set, where M < N;
> an instruction fetch unit coupled to receive instructions from the instruction cache, and operable to produce control signals representative of decoded N-bit instructions; and
> one or more execution units coupled to the receive the control signals from the instruction fetch unit,
> **the instruction fetch unit comprising a translation unit to translate an M-bit instruction received from the instruction cache to produce N-bit instructions, at least one M-bit instruction producing a sequence of N-bit instructions;**
> **the instruction fetch unit further comprising a decoder unit to decode only N-bit instructions, thereby producing the control signals, the translation unit configured to deliver the N-bit instructions to the decoder unit,**
> **wherein the M-bit instruction set includes data instructions that produce results corresponding to M-bit operations,**
> **wherein the N-bit instruction set includes first data instructions that produce results corresponding to N-bit operations and second data instructions that include N-bit instructions not otherwise needed for N-bit operation that emulate M-bit instructions to produce results corresponding to M-bit operations,**
> wherein the instruction fetch unit is configured to produce one or more of the second data instructions in response to receiving an M-bit data instruction

(*emphasis added*). Such limitations are not disclosed by *Jaggar*.

Jaggar discloses the mapping of instruction sets, such as X-bit and Y-bit instructions, where a second instruction set is a subset of a first instruction set, so that a one-to-one mapping is possible between first and second instructions (col. 1, line 34-col. 2, line 17; col. 5, lines 19-28). *Jaggar* does not disclose a single M-bit instruction translation producing a sequence of N-bit instructions upon translation, as *Jagger*

discloses a one-to-one mapping. Further, *Jaggar* does not disclose the N-bit instructions including instructions corresponding to N-bit instructions and M-bit instructions, including N-bit instructions not otherwise needed for N-bit operation that emulate M-bit instructions in order to produce results corresponding to M-bit operations. *Jaggar* instead discloses making the second instruction set a subset of the first instruction set. As *Jaggar* does not disclose these limitations, *Jaggar* cannot anticipate Applicants' claim 27, or the claims that depend therefore. Applicants' other pending claims recite limitations that similarly are not disclosed by *Jaggar*, such that these claims also cannot be anticipated by *Jaggar*.

Claims 27-40 are rejected under 35 U.S.C. §102(b) as being anticipated by *Hammond* (US 5,638,525). Applicants respectfully submit that *Hammond* does not disclose each element of these claims. *Hammond* discloses a system for transitioning between instruction sets, which can be different bit instruction sets (col. 3, line 43-col. 4, line 60). *Hammond* discloses that the processor can switch between modes for the first and second instruction sets (col. 5m lines 9-18), can include separate decoders (col. 11, line 64-col. 12, line 14), and can include a translator for translating instructions between a first and second instruction set (col. 14, line 55-col. 16, line 58). *Hammond* discloses the translation, in part, to utilize a single decoder. *Hammond* does not, however, disclose N-bit instructions including instructions corresponding to N-bit instructions and M-bit instructions, including N-bit instructions not otherwise needed for N-bit operation that emulate M-bit instructions in order to produce results corresponding to M-bit operations. As such, *Hammond* cannot anticipate Applicants claims 27-40.

Applicants therefore respectfully request that the rejections with respect to claims 27-40 be withdrawn.

IV. Amendment to the Claims

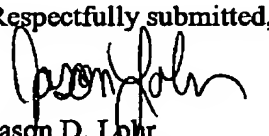
Unless otherwise specified, amendments to the claims are made for purposes of clarity, and are not intended to alter the scope of the claims or limit any equivalents thereof. The amendments are supported by the specification and do not add new matter.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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